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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
AUDUONG, GENE NGHIA	
ART UNIT	**PAPER NUMBER**
2827	

DATE MAILED: 10/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/766,004	NAGRANI ET AL.	
	Examiner	Art Unit	
	Gene N. Auduong	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-17 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-17 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Yomita et al. (U.S. pat. No. 5,457,661).

Regarding claim 6, Tomita et al. disclose a column output delay circuit for a memory device (figure 2, column decoder circuits 121, 122) comprising: a first delay device (figure 2, lower delay device 24 of column device of second stage), the first delay device delaying a column enable signal for a first period of time; and a second delay device (figure 2, upper delay device 24), the second delay device delaying a column enable signal for a second period of time (col. 4, lines 36+).

Regarding claim 7, Tomita et al. disclose the circuit of claim 6, wherein the first delay device delays a sensing operation on an input/output signal line having less capacitance (figure 2, lower delay device 24 to the memory array is shorter than the other), and an accumulation of the first and second delay device delays a sensing operation on an input/output signal line having greater capacitance (see figure 2).

Regarding claim 8, Tomita et al. disclose the circuit of claim 6 further comprising a first column enable signal produced by the first delay device, and a second column enable signal produced by a combination of the first and second delay device (figure 2, column 4, lines 36+).

Claims 9-13 and 14-17 claiming the similar limitation as previously discussed in claims 6-8 but in the alternative way and with the further limitation such as a processor. A processor or controller is a must have limitation in any device to control the various function in the device. Therefore, they are analyzed as previously discussed with respect to claims 6-8.

Regarding claims 1-5, the apparatus as previously discussed in claims 6-8, 9-13 and 14-17 would be performed the method as claimed. Therefore, they are analyzed as previously discussed with respect to apparatus claims 6-8, 9-13 and 14-17.

Response to Arguments

Applicant's arguments filed June 11, 2005 have been fully considered but they are not persuasive.

In re pages 7-8, Applicants argue that "Claim 1 recites, inter alia, 'transferring data from a memory module onto an input/output signal line; and sensing the data based on a capacitance of said input/output signal line'; Yomita teaches a column output delay circuit within each decoder which senses all of the lines corresponding to the decoder simultaneously. However, Yomita does mention or teach a column output circuit for 'sensing the data based on a capacitance of said input/output signal line'".

In response, as set forth in previous office action, Yomita discloses a column output delay circuit for outputting the data from the memory array to the sense circuit via the bitlines, which is the same as "transferring data from a memory module onto an input/output signal line; and sensing the data based on a capacitance of said input/output signal line"; Yomita further teaching that "the output signal has an unignorable delay cause by wiring resistance and wiring capacity and the column decoder, therefore, the column decoder in-need having a predetermine delay

circuit for balancing the output signal from the memory cell array to reduce the problem such as noise so that the access time can be improved", which is the same as "'sensing the data based on a capacitance of said input/output signal line (see Yomita, col. 2, lines 9-21; lines 45-55; col. 5, lines 59-66). Therefore, Yomita patent is clearly teaching the column circuit as claimed

In re page 8, Applicants argue, "Claim 6 is directed to a column output delay circuit in which there is a first and second delay device. Conversely, Yomita teaches a plurality of column output decoders in which each decoder may have a delay circuit. The delay circuits, of each decoder, taught in Yomita do not have "a first delay device, said first delay device delaying a column enable signal for a first period of time; and a second delay device, said second delay device delaying a column enable signal for a second period of time."

In response, as set forth in previous office action, Yomita discloses a column output delay circuit having first delay stage for delaying column enable address for a first predetermined time period, and second delay stage for delaying column enable address for a second predetermined time period to reduce the noise and other problem so that device can be improved in access time and more stable (col. 4, lines 46+; col. 6, lines 49-58), which is the same as claimed "a first delay device, said first delay device delaying a column enable signal for a first period of time; and a second delay device, said second delay device delaying a column enable signal for a second period of time.". Therefore, Yomita patent is clearly teaching the delaying circuit as claimed

In re pages 8-9, Applicants argue that "Claims 9 and 14 recite, inter alia, "a datapath coupled to said memory array by input/output signal lines, and a column output delay circuit, said circuit coupled to sense amplifiers in said datapath for controlling, based on a capacitance of a particular input/output signal line, when the particular input/output signal line is sensed by said

sense amplifiers." Yomita fails to teach a column output delay circuit for controlling when a particular input/output line is sensed.

In response, as set forth in previous office action and as stated by the Applicants' Attorney "Yomita discloses a column output delay circuit having first delay stage for delaying column enable address for a first predetermined time period, and second delay stage for delaying column enable address for a second predetermined time period in which a sense signal is supplied to a latch circuit". Yomita teaching column decoder of first stage and second for delaying the output signals in the first predetermined time period and second predetermined time period which is the same as claimed "a column output delay circuit for controlling when a particular input/output line is sensed". Therefore, Yomita patent is clearly teaching the delaying circuit as claimed.

In re pages 7-9, Applicants argue that "Dependent claims 2-5, 7-9, 10-13 and 15-17 are patentable at least based on their dependency and for the reason discussed in claims 1, 6, 9 and 14".

In response, the examiner considers that claims 2-5 7-9, 10-13 and 15-17, as claimed, still does not distinguish over Yomita patent, teaching the column output circuit having delaying device foe delaying the output enable signals so that the output signals can be obtained at a higher access rate and more stable. Therefore, Yomita patent is clearly anticipated to independent claims 1, 6, 9 and 14; and its dependent claims 2-5, 7-9, 10-13 and 15-17.

It is noted that the features upon which applicant relies (i.e., currents on the bit and word lines under test would vary) are not recited in the rejected claim(s). Although the claims are

interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gene N. Auduong whose telephone number is (571) 272-1773. The examiner can normally be reached on 9-5-4, alternate second Monday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai Ho can be reached on (571) 272-1777. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

GA
September 26, 2005

Gene N Auduong
Primary Examiner
Art Unit 2827